Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-8. (Canceled).

9. (Currently Amended) A dual damascene process comprising:

on a first wiring layer, providing a dielectric layer having an upper surface and a thickness;

forming a via hole that extends from said upper surface to said first wiring layer;

patterning and etching said dielectric layer, thereby forming a trench having a bottom surface, a mouth, and side walls, said trench being disposed so as to fully overlap said via hole and to extend a depth below said upper surface, said depth being greater than a depth of said via hole, wherein the depth of the via hole extends a distance from said trench bottom surface to the first wiring layer;

by means of PVD, depositing a [[seed]] metal-containing layer ~~of metal~~ to coat the dielectric layer; said bottom surface, and said side walls;

reducing the [[seed]] metal-containing layer by an amount to remove any overhang present at the mouth of the trench;

forming a filler layer that overfills the trench and via hole; and

planarizing said filler layer to form a metal conductive via whose aspect ratio is less than about 6:1 whereby its electrical resistance is less than about 1 ohm.

10. (Original) The process described in claim 9 wherein the metal is selected from the group consisting of copper, gold, and silver.

11. (Original) The process described in claim 9 wherein the metal is copper and said electrical resistance is less than about 1 ohm.

12. (Currently Amended) A process for filling an opening, comprising:

providing a power supply having high and low voltage settings;

providing an integrated circuit having an upper surface;

removing a portion of said upper surface to a depth, thereby forming an opening having a bottom surface, a mouth, and side walls;

placing said integrated circuit in a sputtering chamber;

in said sputtering chamber, by connecting a metal target to said power supply, set to high voltage, sputter depositing a [[seed]] metal-containing layer ~~of metal~~ to coat the integrated circuit upper surface, the bottom surface, and the side walls of the opening;

then, in said sputtering chamber, by connecting said integrated circuit to said power supply set to low power and voltage, sputter etching the [[seed]] metal-containing layer, to reduce its thickness by an amount, thereby preferentially removing any overhang present at the mouth of the opening; and

forming an additional metal in said opening.

13. (Currently Amended) The process described in claim 12 wherein said power is between about 1KW and 50KW.

14-27. (Canceled).

28. (New) The process of claim 9, wherein the metal containing layer includes a seed layer and a barrier layer.

29. (New) The process of claim 28, wherein the barrier layer includes at least one of tantalum, tantalum nitride, titanium nitride, and tungsten nitride.

30. (New) A dual damascene process comprising:

providing a dielectric layer;

patterning and etching said dielectric layer to form a trench having a bottom surface, a mouth, and side walls;

depositing a barrier layer to coat the dielectric layer; said bottom surface, and said side walls;

depositing a metal-containing layer over the barrier layer;

reducing the metal-containing layer by an amount to remove any overhang present at the mouth of the trench; and

filling the trench.

31. (New) The process of claim 30, wherein the metal-containing layer includes a seed layer and a barrier layer.

32. (New) The process of claim 30, wherein the barrier layer at least one of tantalum, tantalum nitride, titanium nitride, and tungsten nitride.